19-0836; Rev 1; 8/10

EVALUATION KIT AVAILABLE

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

General Description

The MAX7306/MAX7307 I²C-/SMBus™-compatible, serial-interfaced peripherals feature four level-translating I/Os and operate from a 1.62V to 3.6V power supply. The MAX7307 features a port supply (V_{LA}) that allows level translation on I/O ports to operate from a separate power supply from 1.4V to 5.5V. The MAX7306 features an address select input (AD0) to allow up to four unique slave addresses.

The MAX7306/MAX7307 ports P2, P3, and P4 can be configured as inputs, push-pull outputs, and open-drain outputs. Port P1 can be configured as a general-purpose input, open-drain output, or an open-drain $\overline{INT}$ output. Ports P2 and P3 can be configured as OSCIN and OSCOUT, respectively. The MAX7306/MAX7307 include an internal oscillator for PWM, blink, and key debounce, or to cascade multiple MAX7306/MAX7307s. The external clock can be used to set a specific PWM and blink timing. The $\overline{RST}$ input asynchronously clears the 2-wire interface and terminates a bus lockup involving the MAX7306/MAX7307.

All ports configured as output feature 33-step PWM, allowing any output to be set from fully off, 1/32 to 31/32 duty cycle, to fully on. All output ports also feature LED blink control, allowing blink periods of 1/8 second, 1/4 second, 1/2 second, 1, 2, 4, or 8 seconds. Any port can blink during this period with a 1/16 to 15/16 duty cycle.

The MAX7306/MAX7307 are specified over the -40°C to +125°C temperature range and are available in 10-pin µDFN (2mm x 2mm) and 10-pin µMAX® packages.

Applications

Cell Phones	LCD/Keypad Backlights
System I/O Ports	LED Status Indicators

SMBus is a trademark of Intel Corp.
µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

- **1.4V to 5.5V I/O Level Translation Port Supply (V_{LA})**
- **1.62V to 3.6V Power Supply**
- **Four Individually Configurable GPIO Ports**
  P1 = Open-Drain I/O
  P2, P3, P4 = Push-Pull or Open-Drain I/O
- **Individual 33-Step PWM Intensity Control**
- **Blink Controls with 15 Steps on Outputs**
- **1kHz PWM Period Provides Flicker-Free LED Intensity Control**
- **25mA (max) Port Output Sink Current (100mA max Ground Current)**
- **Inputs Overvoltage Protected Up to 5.5V (V_{LA})**
- **Transition Detection with Optional Interrupt Output**
- **Optional Input Debouncing**
- **$\overline{RST}$ Input Clears Serial Interface, Can Restore Power-Up Default State, and Synchronizes Blink Timing**
- **Oscillator Input and Output Enables Cascading Multiple Devices**
- **Low 0.75µA (typ) Standby Current**

Ordering Information

PART	TOP MARK	PIN-PACKAGE
MAX7306ALB+	AAL	10 µDFN (2mm x 2mm)

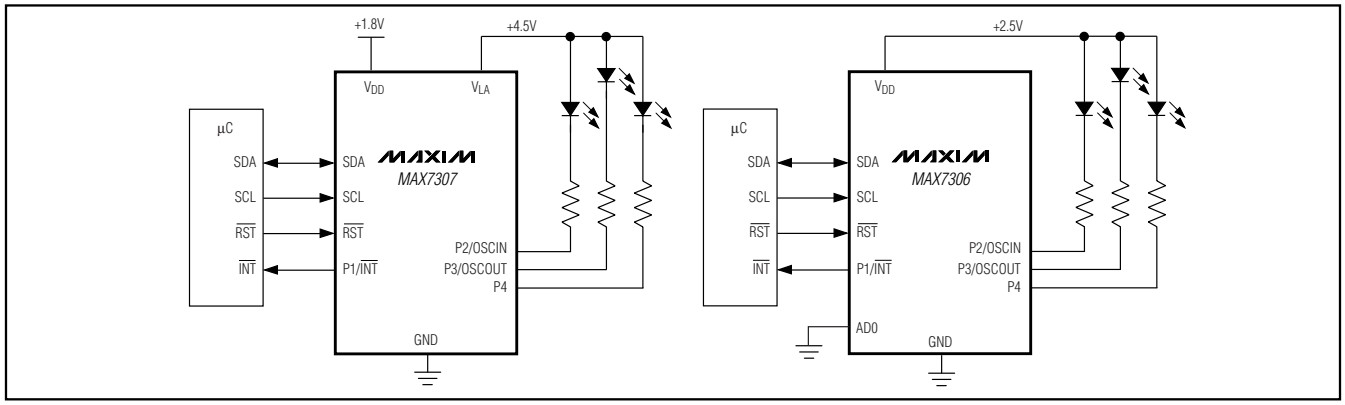
Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Ordering Information continued at end of data sheet.

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} .....-0.3V to +4V
V_{LA}, SCL, SDA, AD0, and $\overline{RST}$.....-0.3V to +6V
P1/$\overline{INT}$, P2/OSCIN, P3/OSCOUT, and P4
MAX7306.....-0.3V to (V_{DD} + 0.3V)
MAX7307.....-0.3V to (V_{LA} + 0.3V)
P1/$\overline{INT}$, P2/OSCIN, P3/OSCOUT, and P4 Sink Current 25mA
P2/OSCIN, P3/OSCOUT, and P4 Source Current 10mA
SDA Sink Current 10mA
V_{DD} Current 10mA
V_{LA} Current (MAX7307) 30mA
GND Current 100mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µDFN (derate 5.0mW/°C over +70°C) 402mW
10-Pin µMAX (derate 10.3mW/°C over +70°C).....825mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX7306)

(V_{DD} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{DD}		1.62		3.60	V
Power-On Reset Voltage	V_{POR}	V_{DD} rising	1.0	1.3	1.6	V
Power-On Reset Hysteresis	$V_{PORHYST}$		10	131	300	mV
Standby Current (Interface Idle)	I_{STB}	Internal oscillator disabled; SCL, SDA, digital inputs at V_{DD} or GND; P1–P4 (as inputs) at V_{DD} or GND		0.75	2	µA
	I_{OSC}	Internal oscillator enabled; SCL, SDA, digital inputs at V_{DD} or GND; P1–P4 (as inputs) at V_{DD} or GND		14	25	
Supply Current (Interface Running)	I_{SUP}	f_{SCL} = 400kHz; other digital inputs at V_{DD} or GND		33	40	µA
Input High Voltage SDA, SCL, AD0	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage SDA, SCL, AD0	V_{IL}				0.3 x V_{DD}	V
Input High Voltage $\overline{RST}$, P1–P4	V_{IHP}		0.7 x V_{DD}			V
Input Low Voltage $\overline{RST}$, P1–P4	V_{ILP}				0.3 x V_{DD}	V
Input Leakage Current SDA, SCL, AD0	I_{IH}, I_{IL}	V_{DD} or GND	-1		+1	µA
Input Leakage Current $\overline{RST}$, P1–P4	I_{IHP}, I_{ILP}	V_{DD} or GND	-1		+1	µA
Input Capacitance SDA, SCL, AD0, P1–P4				8		pF
Output Low Voltage P1–P4	V_{OL}	V_{DD} = 1.62V, I_{SINK} = 3mA		0.06	0.11	V
		V_{DD} = 2.5V, I_{SINK} = 16mA		0.19	0.4	
		V_{DD} = 3.3V, I_{SINK} = 20mA		0.2	0.4	
Output High Voltage P2, P3, and P4	V_{OH}	V_{DD} = 1.62V, I_{SOURCE} = 0.5mA	1.55	1.6		V
		V_{DD} ≥ 2.5V, I_{SOURCE} = 5mA	V_{DD} - 0.3	2.3		
		V_{DD} ≥ 3.3V, I_{SOURCE} = 8mA	V_{DD} - 0.4	3.1		
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			0.3	V

ELECTRICAL CHARACTERISTICS (MAX7307)

(V_{DD} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, V_{LA} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{DD}		1.62		3.60	V
Port Logic Supply Voltage	V_{LA}		1.40		5.50	V
Power-On Reset Voltage	V_{POR}	V_{DD} rising	1.0	1.3	1.6	V
Power-On Reset Hysteresis	$V_{PORHYST}$		10	131	300	V
Standby Current (Interface Idle)	I_{STB}	Internal oscillator disabled; SCL, SDA, digital inputs at V_{DD} or GND; P1–P4 (as inputs) at V_{LA} or GND		0.75	2	µA
	I_{OSC}	Internal oscillator enabled; SCL, SDA, digital inputs at V_{DD} or GND; P1–P4 (as inputs) at V_{LA} or GND		14	25	
Supply Current (Interface Running)	I_{SUP}	f_{SCL} = 400kHz; other digital inputs at V_{LA} or GND		33	40	µA
Port Supply Current (V_{LA})	I_{VLA}	Port (configured as inputs) at V_{LA} or GND		0.05	5	µA
Input High Voltage SDA, SCL, $\overline{RST}$	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage SDA, SCL, $\overline{RST}$	V_{IL}				0.3 x V_{DD}	V
Input High Voltage P1–P4	V_{IHPA}	Input is V_{LA} referred	0.7 x V_{LA}			V
		Input is V_{DD} referred	0.7 x V_{DD}			
Input Low Voltage P1–P4	V_{ILPA}	Input is V_{LA} referred			0.3 x V_{LA}	V
		Input is V_{DD} referred			0.3 x V_{DD}	
Input Leakage Current SDA, SCL, AD0, $\overline{RST}$	I_{IH}, I_{IL}	V_{DD} or GND	-1		+1	µA
Input Leakage Current P1–P4	I_{IHP}, I_{ILP}	V_{LA} or GND	-1		+1	µA
Input Capacitance SDA, SCL, AD0, $\overline{RST}$, P1–P4				8	0.11	pF
Output Low Voltage P1–P4	V_{OL}	V_{DD} = 1.62V, I_{SINK} = 3mA		0.06	0.11	V
		V_{DD} = 2.5V, I_{SINK} = 16mA		0.19	0.4	
		V_{DD} = 3.3V, I_{SINK} = 20mA		0.2	0.4	
Output High Voltage P2, P3, P4	V_{OH}	V_{LA} = 1.62V, I_{SOURCE} = 0.5mA	1.3	1.4		V
		V_{LA} = 2.5V, I_{SOURCE} = 5mA	V_{LA} - 0.3	2.3		
		V_{LA} = 3.3V, I_{SOURCE} = 8mA	V_{LA} - 0.4	3.1		
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			0.3	V

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

PORT, INTERRUPT ($\overline{INT}$), AND RESET ($\overline{RST}$) TIMING CHARACTERISTICS

(V_{DD} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, V_{LA} = 3.3V (MAX7307 only), T_A = +25°C.) (Note 1) (See Figures 14, 15, and 16)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	f_{CLK}	f_{CLK} = internal oscillator		32		kHz
		f_{CLK} = external input			1	MHz
Port Output Data Valid High Time	t_{PPVH}	C_L ≤ 100pF			4	µs
Port Output Data Valid Low Time (Internal or External Oscillator Running)	t_{PPVL1}	C_L ≤ 100pF (Note 2)			1 / f_{CLK}	µs
Port Output Data Valid Low Time (Oscillator Not Running)	t_{PPVL2}	C_L ≤ 100pF		40		µs
Port Input Setup Time	t_{PSU}	C_L = 100pF	0			µs
Port Input Hold Time	t_{PH}	C_L = 100pF	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	C_L = 100pF			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	C_L = 100pF			4	µs
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	t_{RST}		900			ns

TIMING CHARACTERISTICS

(V_{DD} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, V_{LA} = 3.3V (MAX7307 only), T_A = +25°C.) (Note 1) (See Figure 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Timeout	$t_{TIMEOUT}$			31		ms
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU,STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 3)			0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		20 + 0.1C_b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		20 + 0.1C_b	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Note 4)		20 + 0.1C_b	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 2)			400	pF

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design.

Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

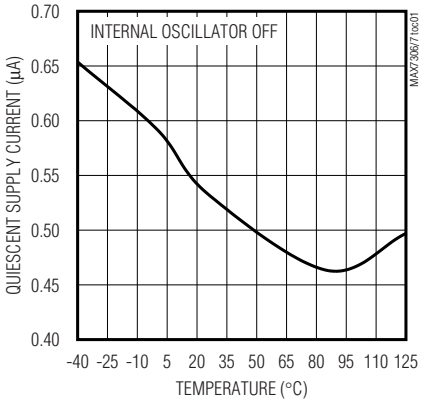
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 x V_{DD} and 0.7 x V_{DD}.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

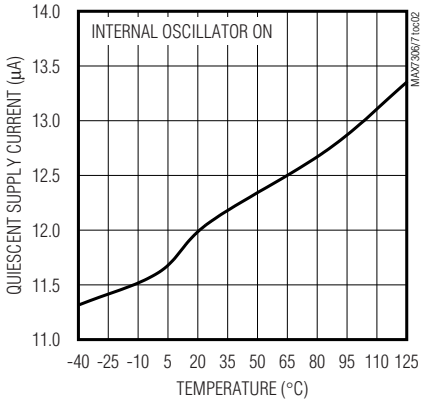
Typical Operating Characteristics

(V_{DD} = 3.3V, V_{LA} = 3.3V, and T_A = +25°C, unless otherwise noted.) (MAX7307)

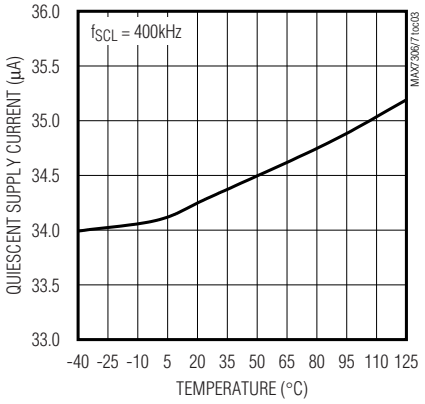
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



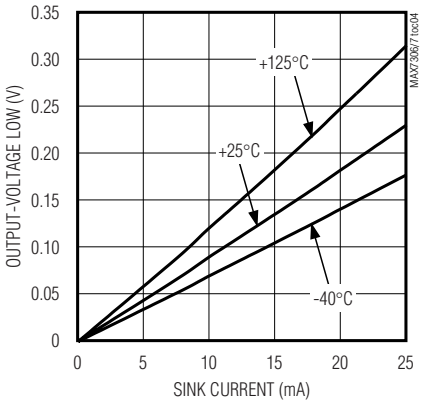
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



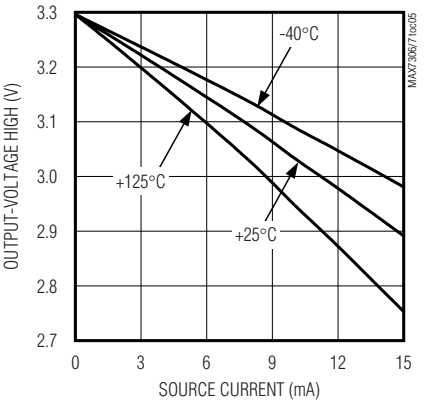
ACTIVE SUPPLY CURRENT vs. TEMPERATURE



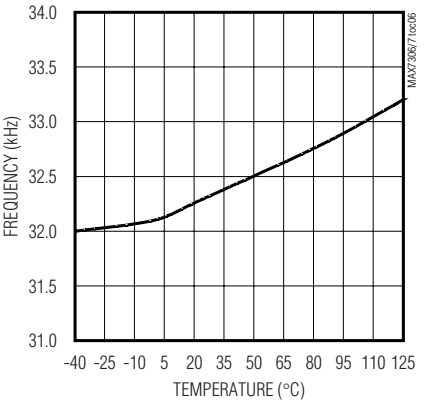
PORT OPEN-DRAIN OUTPUT LOW VOLTAGE vs. SINK CURRENT



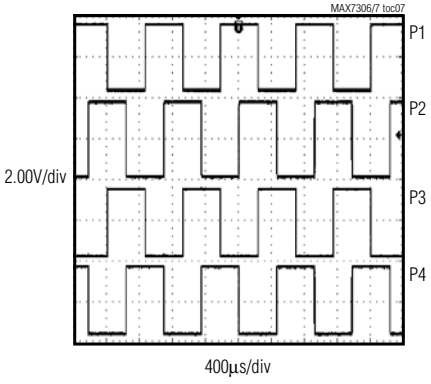
PUSH-PULL OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



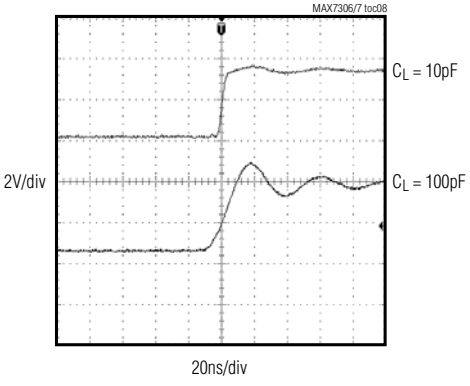
INTERNAL OSCILLATOR vs. TEMPERATURE



STAGGERED PWM OUTPUT



PUSH-PULL OUTPUT RISE TIME

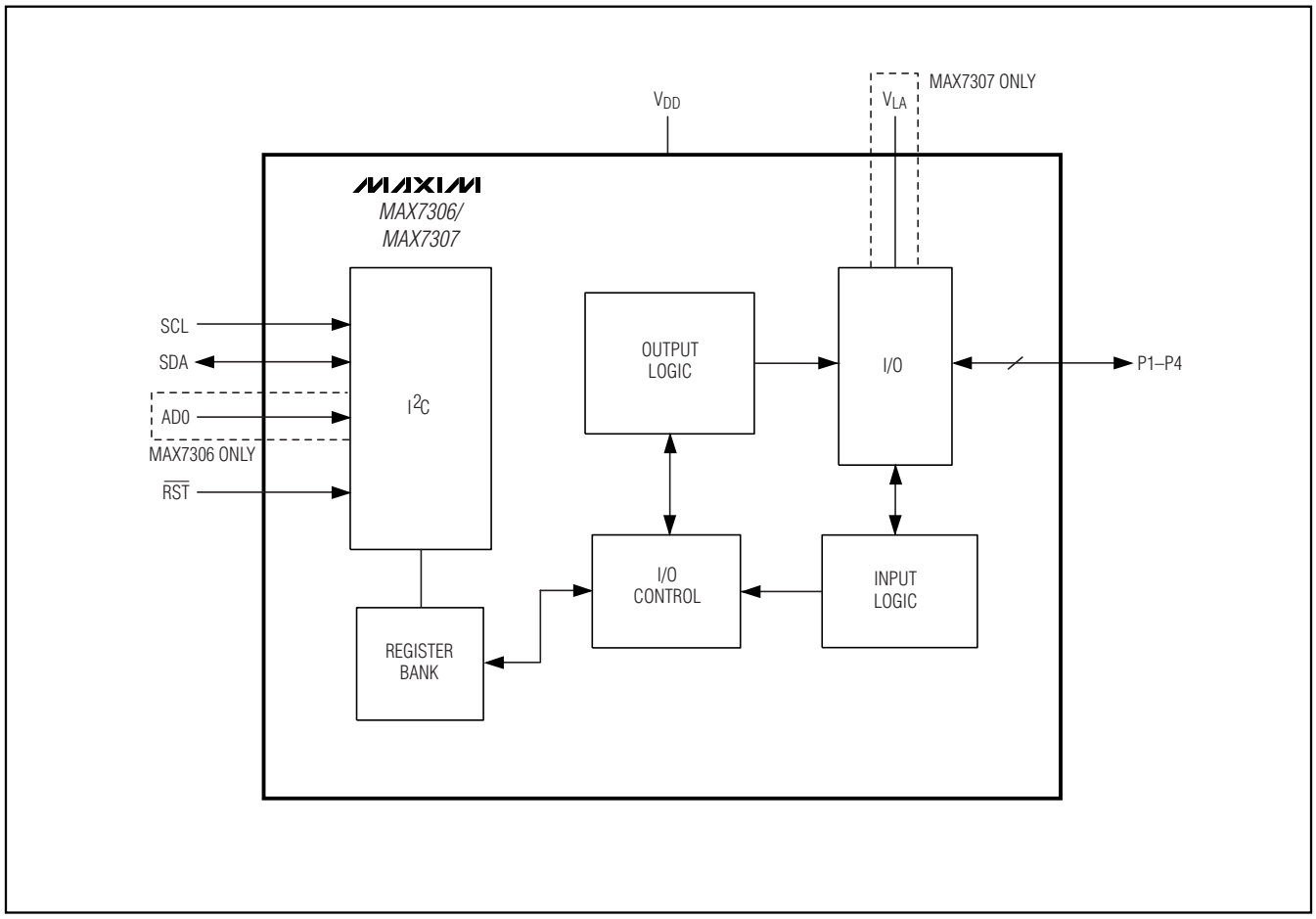


SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

Pin Description

PIN		NAME	FUNCTION
MAX7306	MAX7307		
1	1	$\overline{RST}$	Reset Input. $\overline{RST}$ is an active-low input, referenced to V_{DD}, that clears the 2-wire interface, which can be configured to put the device in the power-up reset condition and reset the PWM and blink timing.
2	2	P1/$\overline{INT}$	Input/Output Port. P1/$\overline{INT}$ is configurable as an open-drain I/O or as a transition detection interrupt output.
3	3	GND	Ground
4	4	P2/OSCIN	Input/Output Port. P2/OSCIN is configurable as a push-pull I/O, open-drain I/O, or as the PWM/blink/timing oscillator input.
5	5	P3/OSCOUT	Input/Output Port. P3/OSCOUT is configurable as a push-pull I/O, open-drain I/O, or as the PWM/blink/timing oscillator output.
6	6	P4	Input/Output Port. P4 is configurable as a push-pull I/O or an open-drain I/O.
—	7	V_{LA}	Port Supply for P1–P4. Connect V_{LA} to a power supply between 1.40V and 5.5V. Bypass V_{LA} to GND with a 0.1µF capacitor.
7	—	AD0	Address Input. Sets the device slave address. Connect to GND, V_{DD}, SCL, or SDA to provide four address combinations.
8	8	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor.
9	9	SDA	Serial-Data I/O
10	10	SCL	Serial-Clock Input
—	—	EP	Exposed Pad (µMAX only). Connect to GND.

Block Diagram



Detailed Description

The MAX7306/MAX7307 4-port, general-purpose port expanders operate from a 1.62V to 3.6V power supply. Ports P2 through P4 can be configured as inputs, push-pull outputs, and open-drain outputs. Port P1 can be configured as an input and an open-drain output; P1 can also be configured to function as an ($\overline{INT}$) output.

Each port configured as an open-drain or push-pull output can sink up to 25mA. Push-pull outputs also have a 10mA source drive capability. The MAX7306/MAX7307 are rated to sink a total of 100mA into any combination of the output ports. Output ports have PWM and blink capabilities, as well as logic drive.

Initial Power-Up

On power-up, the MAX7307 default configuration has all ports configured as input ports with logic levels referenced to V_{LA}. The MAX7306 default configuration has all ports configured as input ports with logic levels referenced to V_{DD}. The transition detection interrupt status flag resets and stays high (see Tables 1 and 2).

Device Configuration Registers

The device configuration registers set up the interrupt function, serial-interface bus timeout, PWM/blink, oscillator options, global blink period, and reset options (see Tables 3 and 4).

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

Table 1. Register Address Map

REGISTER	ADDRESS	AUTOINCREMENT ADDRESS	POR STATE
Port P1 or $\overline{INT}$ Output	0x01	0x02	0x80
Port P2 or OSCIN Input	0x02	0x03	0x80
Port P3 or OSCOUT Output	0x03	0x04	0x80
Port P4	0x04	0x05*	0x80
Configuration 26	0x26	0x27	0xEC
Configuration 27	0x27	0x28*	0x8F
FACTORY RESERVED (Do not write to these registers)	0x3C–0x3F	0x3F–0x40	0x00
FACTORY RESERVED (Do not write to these registers)	0x00	0x01	0x80

**No registers are present.*

Table 2. Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Ports P1–P4	Ports P_ are V_{LA} referred input ports with interrupt and debounce disabled	0x01–0x04	1	0	0	0	0	0	0	0
Configuration 26	$\overline{RST}$ does not reset registers or counters; blink period is 1Hz; transition flag clear; interrupt status flag clear	0x26	1	1	1	0	1	1	0	0
Configuration 27	Ports P1–P4 are GPIO ports; bus timeout is disabled	0x27	1	0	0	0	1	1	1	1

Table 3. Configuration Register (0x26)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION
D7	Interrupt Status Flag (Read-Only)	0	An interrupt has occurred on at least one interrupt enabled input port.
		1*	No interrupt has occurred on an interrupt enabled input port.
D6	Transition Flag (Read-Only)	0	Transition has occurred on an input port.
		1*	No transition has occurred on an input port.
D5	Reserved	0	Reserved.
D4, D3, D2	Blink Prescaler Bits	0/1	See Table 9 for blink frequency setting.
D1	$\overline{RST}$ Timer	0*	$\overline{RST}$ does not reset PWM/blink counters.
		1	$\overline{RST}$ resets PWM/blink counters.
D0	$\overline{RST}$ POR	0*	$\overline{RST}$ does not reset registers to power-on-reset state.
		1	$\overline{RST}$ resets registers to power-on-reset state.

**Default state.*

Table 4. Configuration Register (0x27)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION
D7	Bus Timeout	0	Enables the bus timeout feature.
		1*	Disables the bus timeout feature.
D6, D5, D4	Reserved	0	Reserved.
D3	P3/OSCOUT	0	Sets P3 to output the oscillator.
		1*	Sets P3 as a GPIO controlled by register 0x03.
D2	P2/OSCIN	0	Sets P2 as the oscillator input.
		1*	Sets P2 as a GPIO controlled by register 0x02.
D1	P1/$\overline{INT}$ Output	0	Sets P1 as the interrupt output.
		1*	Sets P1 as a GPIO controlled by register 0x01.
D0	Input Transition	0	Set to 0 on power-up for proper transition detection.

**Default state.*

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

Slave Address

The MAX7307 is set to slave address 0x98 and the MAX7306 can be set to one of four I²C slave addresses 0x98 to 0x9F, using the address input AD0 (see Table 5) and is accessed over an I²C or SMBus serial interface. The MAX7306 slave address is determined on each I²C transmission, regardless of the transmission actually addressing the device or not. The MAX7306 distinguishes whether address input AD0 is connected to SDA, SCL, V_{DD}, or GND during the transmission. Therefore, the MAX7306 slave address can be configured dynamically in an application without toggling the device supply.

Table 5. Slave-Address Selection

AD0 CONNECTION	DEVICE ADDRESS							
	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
GND	1	0	0	1	1	0	0	0/1
V_{DD}	1	0	0	1	1	0	1	0/1
SCL	1	0	0	1	1	1	0	0/1
SDA	1	0	0	1	1	1	1	0/1

I/O Port Registers

The port I/O registers set the I/O ports, one register per port (see Tables 6 and 7). Use the I/O port registers to configure the ports individually as inputs, open-drain, or push-pull outputs. Port P1 can only be configured as an input or an open-drain output. The push-pull bit (D6) setting for the port I/O register P1 is ignored.

I/O Input Port

Configure a port as an input by writing a logic-high to the MSB (bit D7) of the port I/O register (see Table 6). To obtain the logic level of the port input, read the port I/O register bit, D0. This readback value is the instantaneous logic level at the time of the read request if debounce is disabled for the port (port I/O register bit D2 = 0), or the debounced result if debounce is enabled for the port (port I/O register bit D2 = 1). See Figure 1 for input port structure.

I/O Output Port

Configure a port as an output by writing a logic-low to the MSB (bit D7) of the port I/O register. The device reads back the logic level, PWM, or the blink setting of the port (see Table 7).

Table 6. Port I/O Registers (I/O Port Set as an Input, Registers 0x01 to 0x04)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION
D7	Port I/O Set Bit	1	Sets the I/O port as an input.
D6*	Port Supply Reference	0	Refers the input to the V_{LA} supply voltage.
		1	Refers the input to the V_{DD} supply voltage.
D5	Transition Interrupt Enable	0	Disables the transition interrupt.
		1	Enables the transition interrupt.
D4, D3	**Reserved**	**0**	**Do not write to these registers.**
D2	Debounce	0	Disables debouncing of the input port.
		1	Enables debouncing of the input port.
D1	Port Transition State (Read-Only)	0	No transition has occurred since the last port read.
		1	A transition has occurred since the last port read.
D0	Port Status (Read-Only)	0	Port input is logic-low.
		1	Port input is logic-high.

**Bit D6 controls the I/O's supply reference for the MAX7307. The MAX7306 ignores bit D6.*

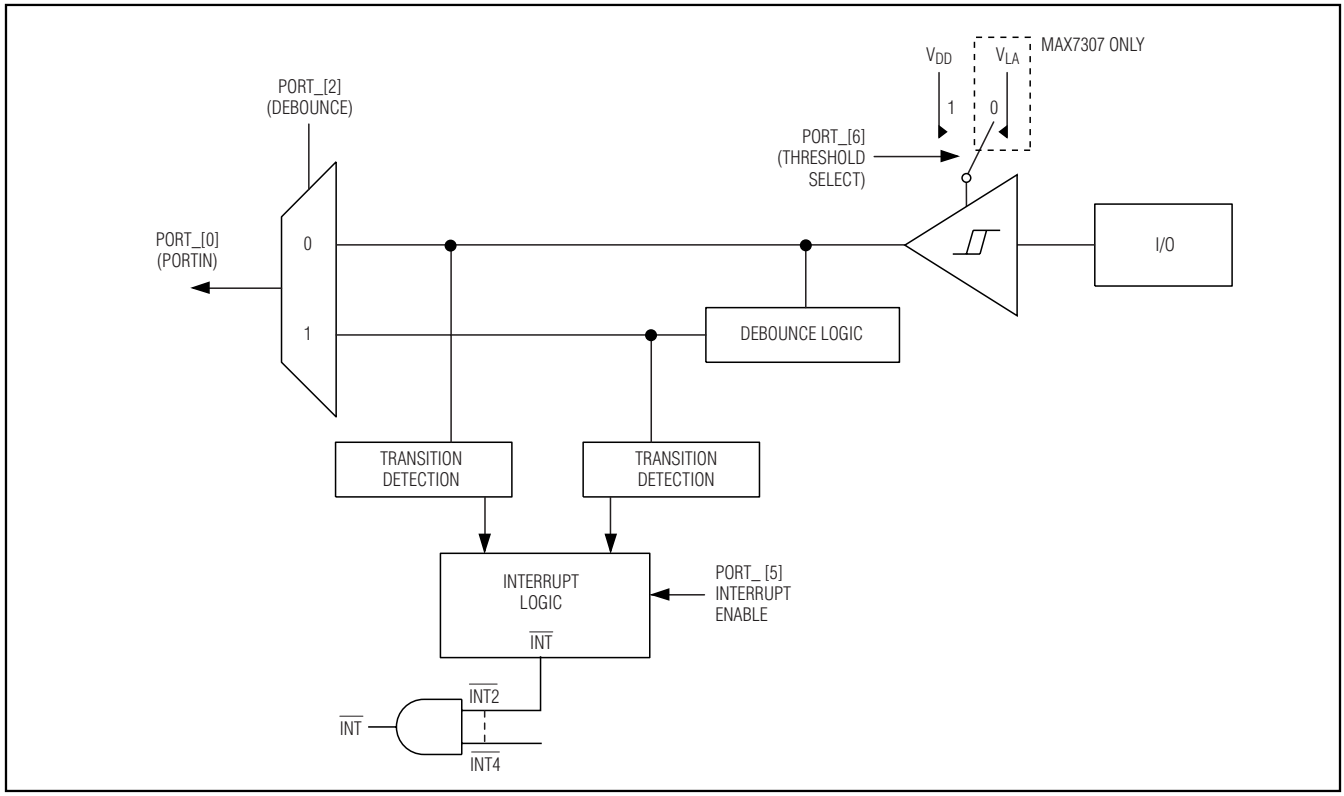


Figure 1. Input Port Structure

Table 7. Port I/O Registers (I/O Port Set as an Output, Registers 0x01 to 0x04)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION
D7	Port I/O Set Bit	0	Sets the I/O port as an output.
D6	Output Port Set to Push-Pull or Open-Drain	0	Sets the output type to open-drain.
		1	Sets the output type to push-pull.
D5	PWM/Blink Enable	0	Sets the output to PWM mode.
		1	Sets the output to blink mode.
D4	Duty Cycle Bit 4	0	MSB of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
		1	MSB of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
D3	Duty Cycle Bit 3	0	Bit 3 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
		1	Bit 3 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
D2	Duty Cycle Bit 2	0	Bit 2 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
		1	Bit 2 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
D1	Duty Cycle Bit 1	0	Bit 1 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
		1	Bit 1 of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
D0	Duty Cycle Bit 0	0	LSB of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.
		1	LSB of the 5-bit duty cycle setting. See the *PWM and Blink Timing* section.

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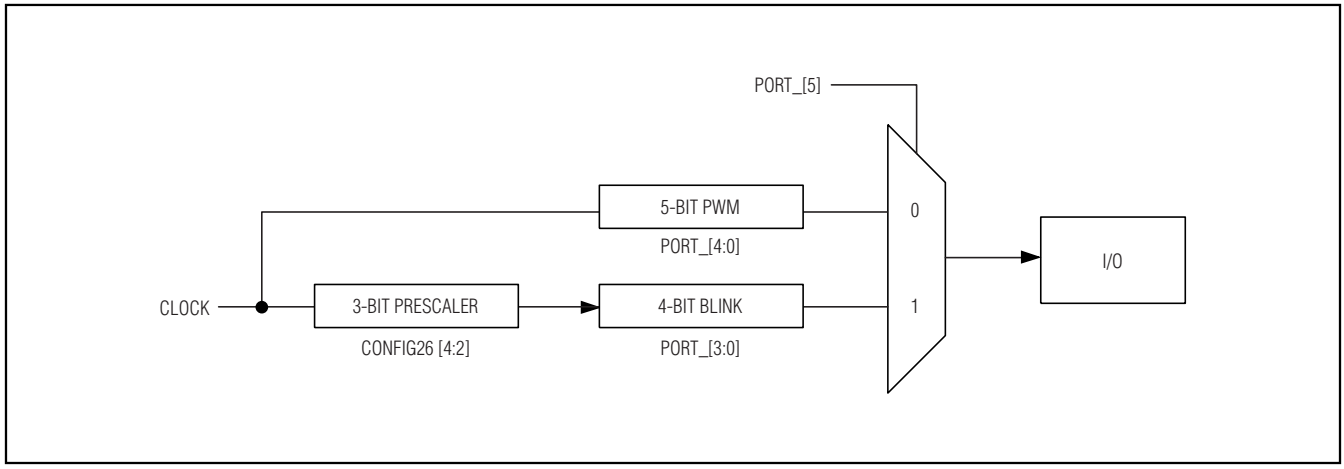

Figure 2. Output Port Structure

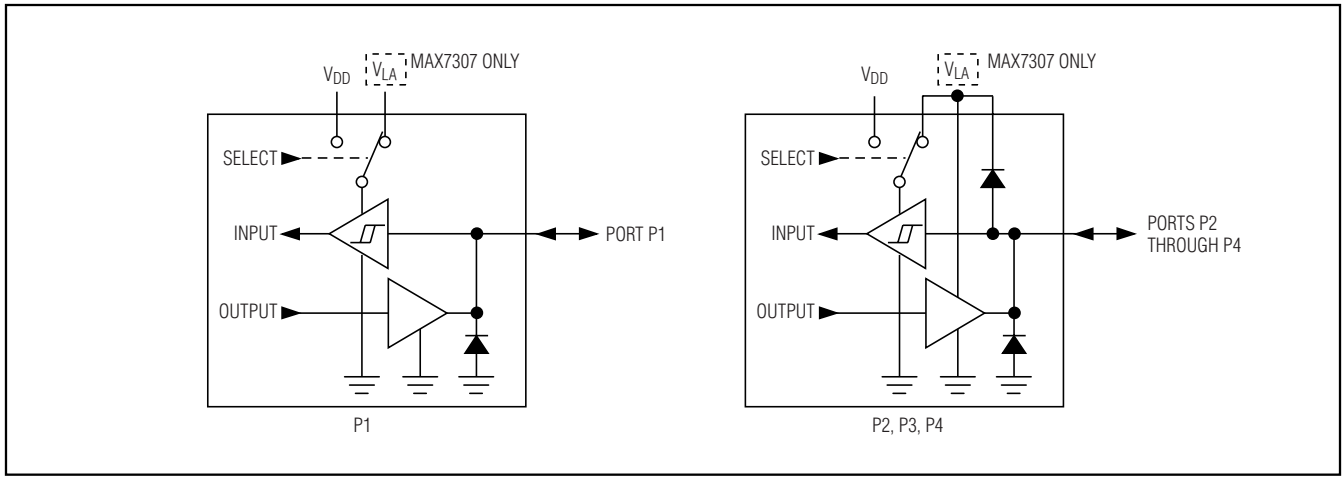

Figure 3. Port I/O Structure

Port Supplies and Level Translation

The MAX7307 features a port supply, V_{LA}, that provides the logic supplies to all push-pull I/O ports. P2 through P4 can be configured as push-pull I/O ports (see Figure 3). V_{LA} powers the logic-high port output voltage sourcing the logic-high port load current. V_{LA} provides level translation capability for the outputs and operates over a 1.40V to 5.5V voltage independent of the power-supply voltage, V_{DD}.

Each port of the MAX7307 set as an input can be configured to switch midrail of either the V_{DD} or the V_{LA} port supplies. Whenever the port supply reference is changed from V_{DD} to V_{LA}, or vice versa, read the port register to clear any transition flag on the port.

Ports P2 through P4 are overvoltage protected to V_{LA}. This is true even for a port used as an input with a V_{DD} port logic-input threshold. Port P1 is overvoltage protected to 5.5V, independent of V_{DD} and V_{LA} (see Figure 3). To mix logic outputs with more than one voltage swing on a group of ports using the same port supply, set the port supply voltage (V_{LA}) to be the highest output voltage. Use push-pull outputs and port P1 for the highest voltage ports, and use open-drain outputs with external pullup resistors for the lower voltage ports. For the MAX7307, when P2, P3, and P4 ports are acting as an input referenced to V_{DD}, make sure the V_{LA} voltage is greater than V_{DD} - 0.3V.

Input Debounce

The MAX7306/MAX7307 sample the input ports every 31ms if input debouncing is enabled for an input port (D2 = 1 of the port I/O register). The MAX7306/MAX7307 compare each new sample with the previous sample. If the new sample and the previous sample have the same value, the corresponding internal register updates.

When the port input is read through the serial interface, the MAX7306/MAX7307 do not return the instantaneous backing value of the logic level from the port because debounce is active. Instead, the MAX7306/MAX7307 return the stored debounced input signal.

When debouncing is enabled for a port input, transition detection applies to the stored debounced input signal value, rather than to the instantaneous value at the input. This process allows for useful transition detection of noisy signals, such as keyswitch inputs, without causing spurious interrupts.

Port Input Transition Detection and Interrupt

Any transition on ports configured as inputs automatically set the D1 bit of that port's I/O registers high. Any input can be selected to assert an interrupt output indicating a transition has occurred at the input port(s). The MAX7306/MAX7307 sample the port input (internally latched into a snapshot register) during a read access to its port P_ I/O register. The MAX7306/MAX7307 continuously compare the snapshot with the port's input condition. If the device detects a change for any port input, an internal transition flag sets for that port. Read register 0x26 to clear the interrupt, then read all the port I/O registers (0x01 to 0x04) by initiating a burst read to clear the MAX7306/MAX7307's internal transition flag. Note that when debouncing is enabled for a port input, transition detection applies to the stored debounced input signal value, rather than to the instantaneous value at the input. Transition bits D4 and D3 of port registers must be set to 0 to detect the next rising or falling edge on the input port (P_).

The MAX7306/MAX7307 allow the user to select the input port(s) that cause an interrupt on the $\overline{INT}$ output. Set $\overline{INT}$ for each port by using the $\overline{INT}$ enable bit (bit D5) in each port P_ register. The appropriate port's transition flag always sets when an input changes, regardless of the port's $\overline{INT}$ enable bit settings. The $\overline{INT}$ enable bits allow processor interrupt only on critical events, while the inputs and the transition flags can be polled periodically to detect less critical events. When debounce is disabled, a signal transition between the 9th and 11th falling edges of the clock will not be registered, since the transition is detected and cleared at the same time.

Ports configured as outputs do not feature transition detection, and therefore, cannot cause an interrupt.

The $\overline{INT}$ output never reasserts during a read sequence because this process could cause a recursive reentry into the interrupt service routine. Instead, if a data change occurs during the read that would normally set the $\overline{INT}$ output, the interrupt assertion is delayed until the STOP condition. If the changed input data is read before the STOP condition, a new interrupt is not required and not asserted. The $\overline{INT}$ bit and $\overline{INT}$ output (if selected) have the same value at all times.

Transition Flag

The transition bit in device configuration register 0x26 is a NOR of all the port I/O registers' individual transition bits. A port's I/O register's transition bit sets when that port is set as an input, and the input changes from the port's I/O registers last read through the serial interface. A port's individual transition bit clears by reading that port's I/O register. Always write a 0 to bits D4 and D3 of the configuration register 0x26 to properly configure a transition detection. The transition flag of configuration register 0x26 is only cleared after reading all ports I/O registers on which a transition has ocurred.

$\overline{RST}$ Input

The active-low $\overline{RST}$ input operates as a hardware reset that voids any ongoing I²C transition involving the MAX7306/MAX7307 (this feature allows the MAX7306/MAX7307 supply current to be minimized in power-critical applications by effectively disconnecting the MAX7307 from the bus). $\overline{RST}$ also operates as a chip enable, allowing multiple devices to use the same I²C slave address if only one MAX7306/MAX7307 has its $\overline{RST}$ input high at any time. $\overline{RST}$ can be configured to restore all port registers to the power-up settings by setting bit D0 of device configuration register 0x26 (Table 1). $\overline{RST}$ can also be configured to reset the internal timing counters used for PWM and blink by setting bit D1 of device configuration register 0x26.

When $\overline{RST}$ is low, the MAX7306/MAX7307 are forced into the I²C STOP condition. The reset action does not clear the interrupt output $\overline{INT}$.

The $\overline{RST}$ input is referenced to V_{DD} and is overvoltage tolerant up to the supply voltage, V_{LA}.

$\overline{INT}$ Output

Port P1 can be configured as a latching interrupt output, $\overline{INT}$, that flags any transients on any combination of selected ports configured as inputs. Any transitions occurring at the selected inputs assert $\overline{INT}$ low to alert

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the host processor of data changes at the selected inputs. Reset $\overline{INT}$ by reading any port's I/O registers (0x01 to 0x04).

Standby Mode

Upon power-up, the MAX7306/MAX7307 enter standby mode when the serial interface is idle. If any of the PWM intensity control, blink, or debounce features are used, the operating current rises because the internal PWM oscillator is running and toggling counters. When using OSCIN to override the internal oscillator, the operating current varies according to the frequency at OSCIN. When the serial interface is active, the operating current also increases because the MAX7306/MAX7307, like all I²C slaves, have to monitor every transmission. The bus timeout circuit and debounce circuit use the internal oscillator even if OSCIN is selected.

Internal Oscillator and OSCIN/OSCOUT External Clock Options

The MAX7306/MAX7307 contain an internal oscillator nominally at 32kHz. The MAX7306/MAX7307 always use the internal oscillator for bus timeout and for debounce timing (when enabled). The internal oscillator is also used by default to generate PWM and blink timing. The internal oscillator only runs when the clock output OSCOUT is needed to keep the operating current as low as possible.

The MAX7306/MAX7307 can use an external clock source instead of the internal oscillator for the PWM and blink timing. The external clock can range from DC to 1MHz and it connects to the P2/OSCIN port. The P3/OSCOUT port provides a buffered and level-shifted output of the internal oscillator or external clock to drive other devices. Select the P2/OSCIN and P3/OSCOUT port options using the device configuration register 0x27 bits D2 and D3 (see Table 2).

The P2/OSCIN port is overvoltage protected to supply voltage V_{LA} for the MAX7307, so the external clock can exceed V_{DD} if V_{LA} is greater than V_{DD}. The external clock cannot exceed V_{DD} for the MAX7306. The port P2 register (see Tables 2 and 6) sets the P2/OSCIN logic threshold (30%/70%) to either the V_{DD} supply or the V_{LA}.

Use OSCOUT or an external clock source to cascade up to four MAX7306s per master for applications requiring additional ports. To synchronize the blink action across multiple MAX7306s (see Figures 4 and 5), use OSCOUT from one MAX7306 to drive OSCIN of the other MAX7306s. This process ensures the same blink frequency of all the devices, but also make sure to synchronize the blink phase. The blink timing of multiple MAX7306s is synchronous at the instant of power-up because the blink and PWM counters clear by each device's internal reset circuit, and by default the device's internal oscillators are off upon power-up.

Ensure that the blink phase of all the devices remains synchronized by programming the OSCIN and OSCOUT functionality before programming any feature that causes a MAX7306's internal oscillator to operate (blink, PWM, bus timeout, or key debounce). Configure the $\overline{RST}$ input to reset the internal timing counters used for PWM and blink by setting bit D1 of device configuration register 0x26 (see Table 3).

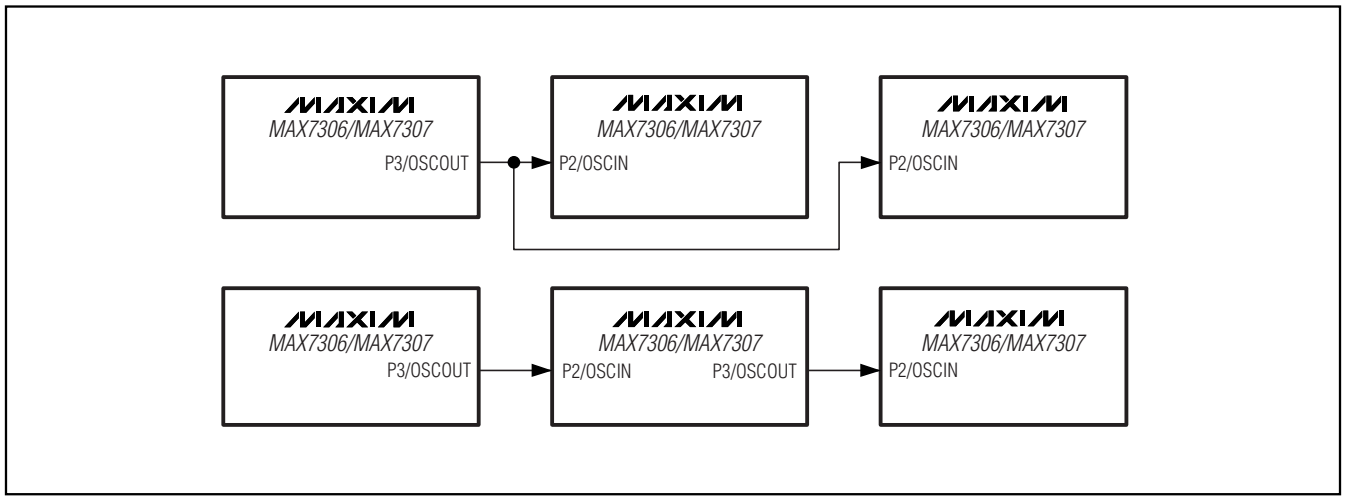

Figure 4. Synchronizing Multiple MAX7306/MAX7307s (Internal Oscillator)

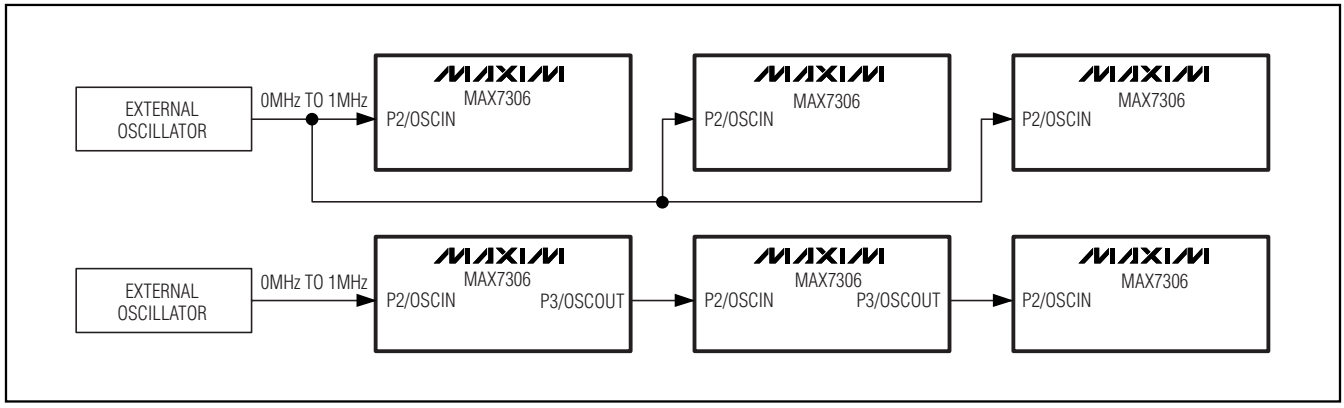

Figure 5. Synchronizing Multiple MAX7306s (External Clock)

PWM and Blink Timing

The MAX7306/MAX7307 divide the 32kHz nominal internal oscillator OSC or external clock source OSCIN frequency by 32 to provide a nominal 1kHz PWM frequency. Use the reset function to synchronize multiple MAX7306s that are operating from the same OSCIN, or to synchronize a single MAX7306/MAX7307's blink timing to an external event. Configure the $\overline{RST}$ input to reset the internal timing counters used by PWM and blink by setting bit D1 of the device configuration register 0x26 (see Table 3).

The MAX7306/MAX7307 use the internal oscillator by default. Configure port P2 using device configuration register 0x27 bit D2 (see Table 4) as an external clock source input, OSCIN, if the application requires a particular or more accurate timing for the PWM or blink functions. OSCIN only applies to PWM and blink; the MAX7306/MAX7307 always use the internal oscillator for debouncing and bus timeout. OSCIN can range up to 1MHz. Use device configuration register 0x27 bit D3 (see Table 2) to configure port P3 as OSCOUT to output a MAX7306/MAX7307's clock. The MAX7306/MAX7307 buffer the clock output of either the internal oscillator OSC or the external clock source OSCIN, according to port D2's setup. Synchronize multiple MAX7306s without using an external clock source input by configuring one MAX7306 to generate OSCOUT from its internal clock, and use this signal to drive the remaining MAX7306s' OSCIN.

A PWM period contains 32 cycles of the nominal 1kHz PWM clock (see Figure 6). Set ports individually to a PWM duty cycle between 0/32 and 31/32. For static logic-level low output, set the ports to 0/32 PWM, and for static logic-level high output, set the port register to 0111xxxx (see Table 8). The MAX7306/MAX7307 stagger the PWM timing of the 4-port outputs, in single or dual ports, by 1/8 of the PWM period. These phase shifts distribute the port-output switching points across the PWM period (see Figure 7). This staggering reduces the di/dt output-switching transient on the supply and also reduces the peak/mean current requirement.

All ports feature LED blink control. A global blink period of 1/8 second, 1/4 second, 1/2 second, 1, 2, 4, or 8 seconds applies to all ports. See Table 9. Any port can blink during this period with a 1/16 to 15/16 duty cycle, adjustable in 1/16 increments. See Table 10. For PWM fan control, the MAX7306/MAX7307 can set the blink frequency to 32Hz.

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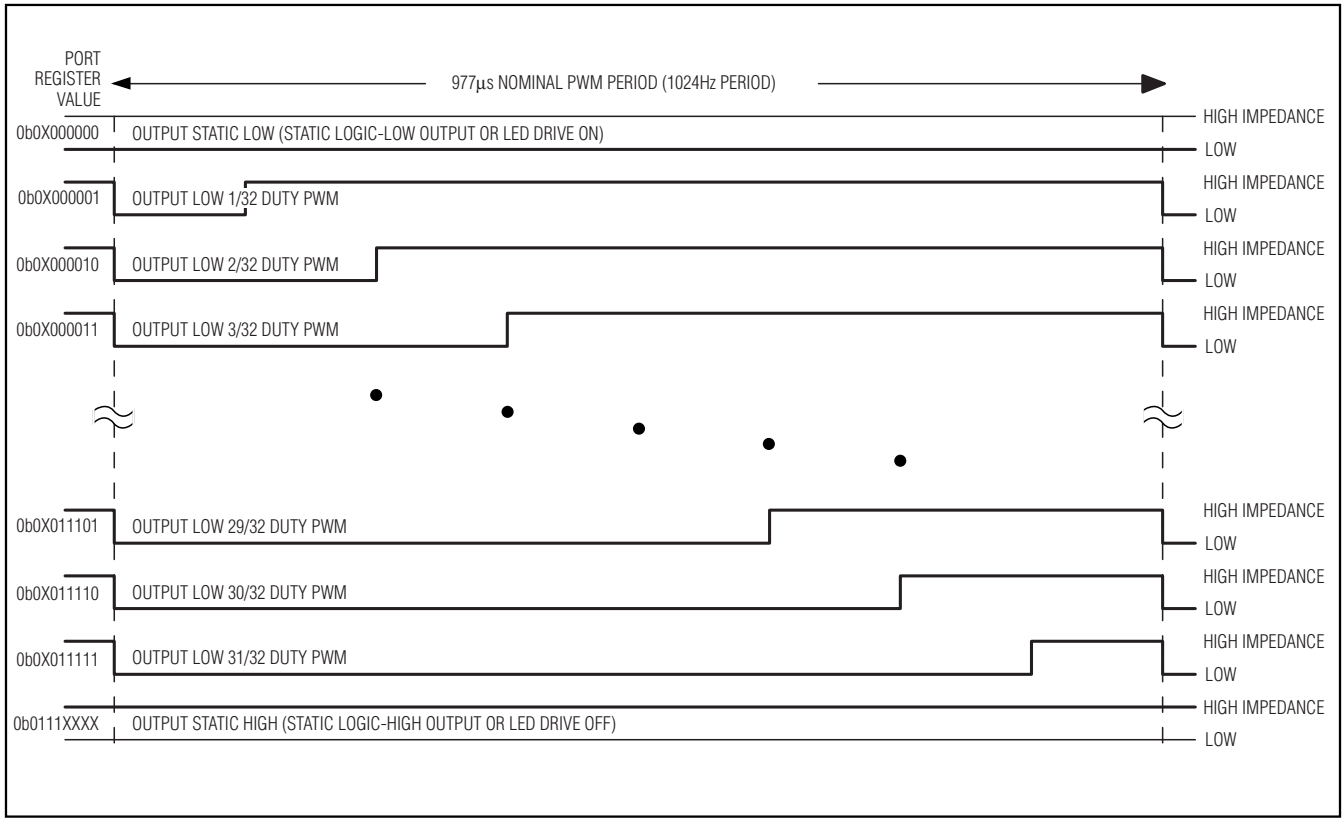

Figure 6. Static and PWM Port Output Waveforms

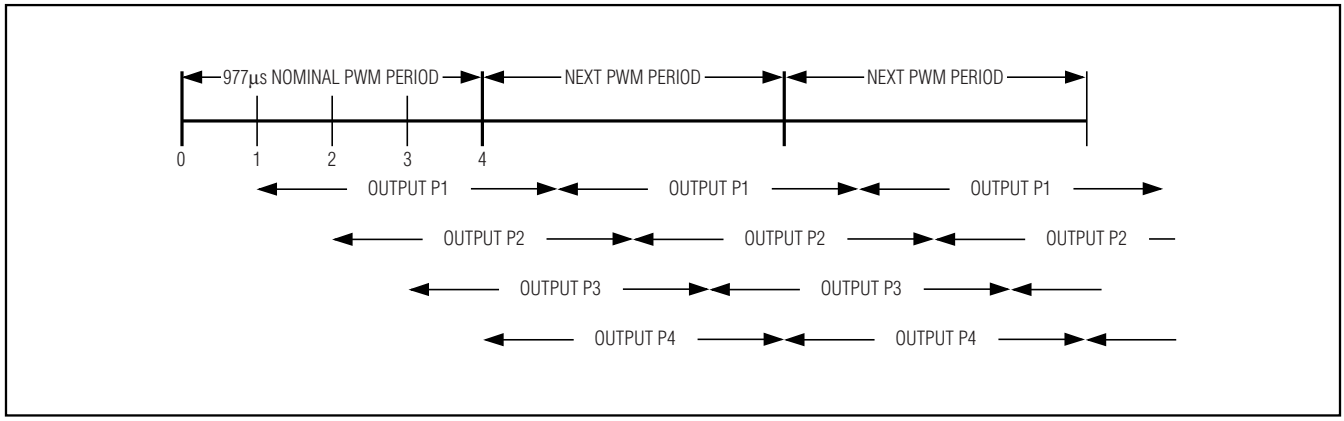

Figure 7. Staggered PWM Phasing Between Port Outputs

Table 8. PWM Settings on Output Ports

PWM SETTING	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Port P_ is a static logic-level low output port	0	X	0	0	0	0	0	0
Port P_ is a PWM output port; PWM duty cycle is 1/32	0	X	0	0	0	0	0	1
Port P_ is a PWM output port; PWM duty cycle is 3/32	0	X	0	0	0	0	1	1
Port P_ is a PWM output port; PWM duty cycle is 7/32	0	X	0	0	0	1	1	1
Port P_ is a PWM output port; PWM duty cycle is 15/32	0	X	0	0	1	1	1	1
Port P_ is a PWM output port; PWM duty cycle is 31/32	0	X	0	1	1	1	1	1
Port P_ is a static logic-level high output port	0	1	1	1	X	X	X	X

Table 9. Blink and PWM Frequencies

BLINK OR PWM SETTING	DEVICE CONFIGURATION REGISTER 0x66			BLINK OR PWM FREQUENCY (32kHz INTERNAL OSCILLATOR) (Hz)	BLINK OR PWM FREQUENCY (0Hz TO 1MHz EXTERNAL OSCILLATOR)
	BIT D4 BLINK2	BIT D3 BLINK1	BIT D2 BLINK0		
Blink period is 8 seconds (0.125Hz)	0	0	0	0.125	OSCIN / 262,144
Blink period is 4 seconds (0.25Hz)	0	0	1	0.25	OSCIN / 131,072
Blink period is 2 seconds (0.5Hz)	0	1	0	0.5	OSCIN / 65,536
Blink period is 1 second (1Hz)	0	1	1	1	OSCIN / 32,768
Blink period is a 1/2 second (2Hz)	1	0	0	2	OSCIN / 16,384
Blink period is a 1/4 second (4Hz)	1	0	1	4	OSCIN / 8192
Blink period is an 1/8 second (8Hz)	1	1	0	8	OSCIN / 4096
Blink period is a 1/32 second (32Hz)	1	1	1	32	OSCIN / 1024
PWM	X	X	X	1024	OSCIN / 32

Table 10. Blink Settings on Output Ports

BLINK SETTINGS	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Port P_ is a static logic-level low output port	0	X	1	0	0	0	0	0
Port P_ is a blinking output port; blink duty cycle is 1/16	0	X	1	0	0	0	0	1
Port P_ is a blinking output port; blink duty cycle is 3/16	0	X	1	0	0	0	1	1
Port P_ is a blinking output port; blink duty cycle is 7/16	0	X	1	0	0	1	1	1
Port P_ is a blinking output port; blink duty cycle is 15/16	0	X	1	0	1	1	1	1
Port P_ is a static logic-level high output port	0	1	1	1	X	X	X	X

X = Don't care.

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Serial Interface

Serial Addressing

The MAX7306/MAX7307 operate as a slave that sends and receives data through an I²C-compatible, 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7306/MAX7307 and generates the SCL clock that synchronizes the data transfer (see Figure 8).

The MAX7306/MAX7307 SDA line operates as both an input and an open-drain output. A 4.7kΩ (typ) pullup resistor is required on SDA. The MAX7306/MAX7307 SCL line operates only as an input. A 4.7kΩ (typ) pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (see Figure 9) sent by a master, followed by the MAX7306/MAX7307 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition (see Figure 9).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (see Figure 9).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (see Figure 10).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to acknowledge receipt of each byte of data (see Figure 11). Thus, each effectively transferred byte requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7306/MAX7307, the devices generate the acknowledge bit because the MAX7306/MAX7307 are the

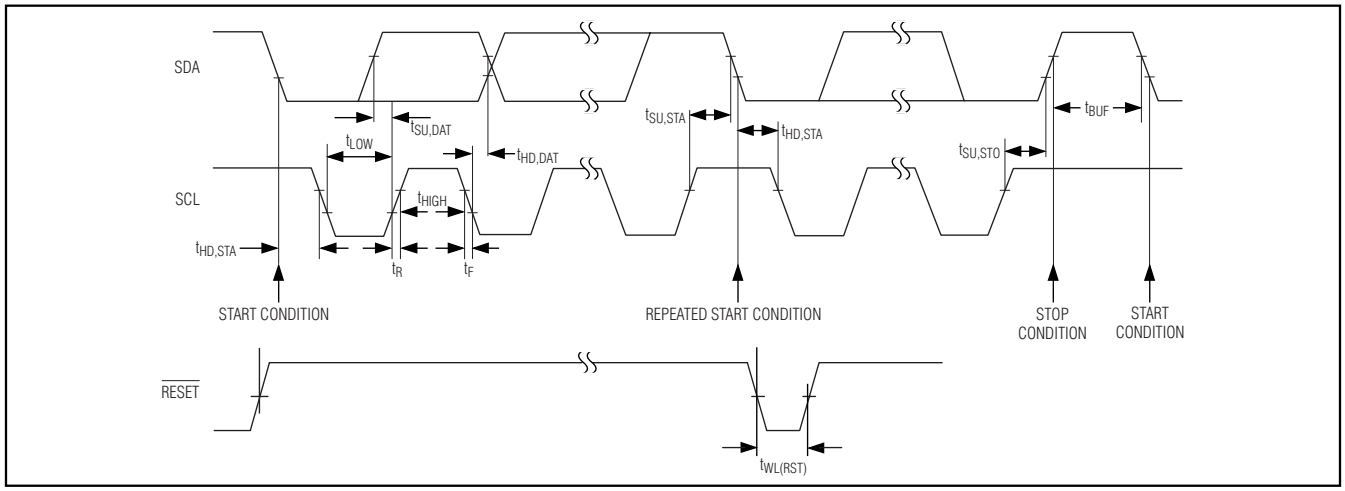

Figure 8. 2-Wire Serial Interface Timing Details

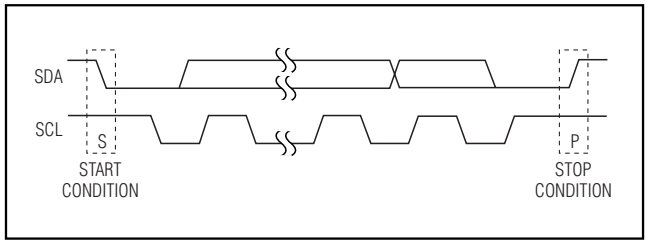

Figure 9. Start and Stop Conditions

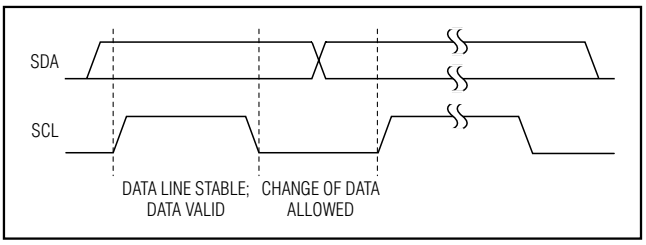

Figure 10. Bit Transfer

recipients. When the MAX7306/MAX7307 transmit to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7306/MAX7307 have a 7-bit long slave address (Figure 12). The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. Set the R/$\overline{W}$ bit low for a write command and high for a read command.

The first 5 bits of the MAX7306 slave address (A6–A2) are always 1, 0, 0, 1, and 1. Slave address bits A1 and A0 are selected by the address input AD0. AD0 can be connected to GND, V_{DD}, SDA, or SCL. The MAX7306 has four possible slave addresses (see Table 5), and therefore, a maximum of four MAX7306 devices can be controlled independently from the same interface. The MAX7307 features a permanent slave address of 0x98.

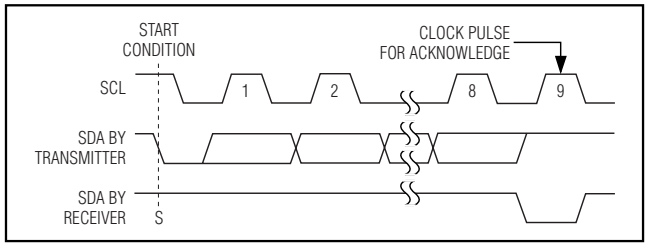

Figure 11. Acknowledge

Message Format for Writing to the MAX7306/MAX7307

A write to the MAX7306/MAX7307 comprises the transmission of the MAX7306/MAX7307's slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7306/MAX7307 is to be written to by the next byte, if received (see Table 1). If a STOP condition is detected after the command byte is received, the MAX7306/MAX7307 take no further action beyond storing the command byte (see Figure 13).

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX7306/MAX7307 selected by the command byte (see Figure 14). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7306/MAX7307 internal registers because the command byte address autoincrements (see Table 1).

Message Format for Reading

The MAX7306/MAX7307 are read using the MAX7306/MAX7307's internally stored command byte as an address pointer the same way the stored command byte is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the

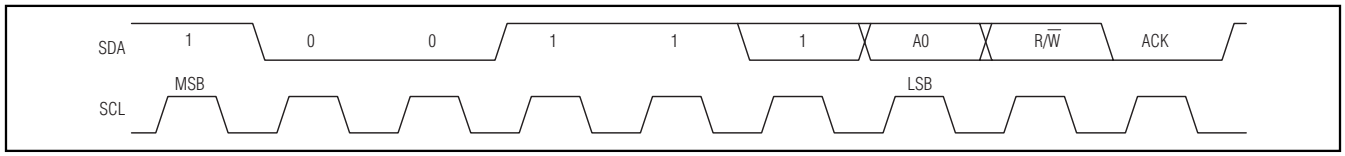

Figure 12. Slave Address

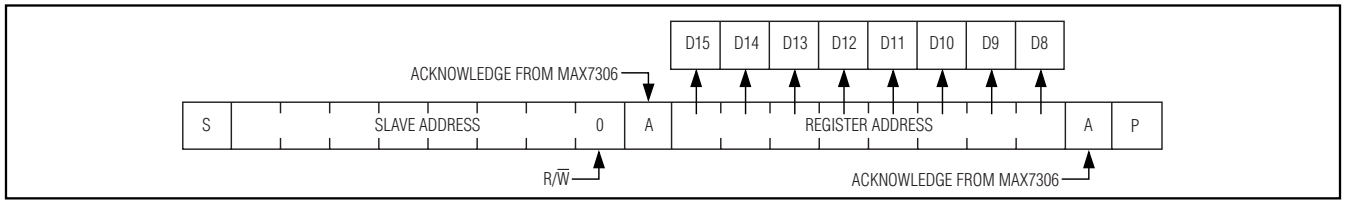

Figure 13. Register Address Received

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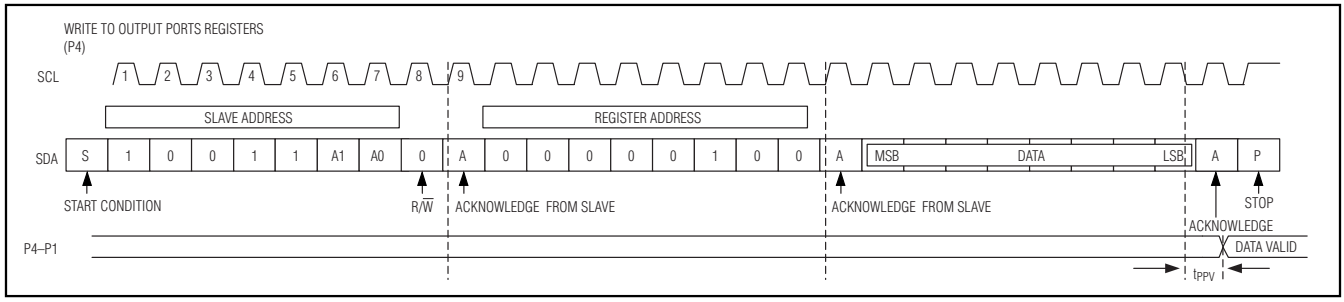


Figure 14. Write to Output Port Registers

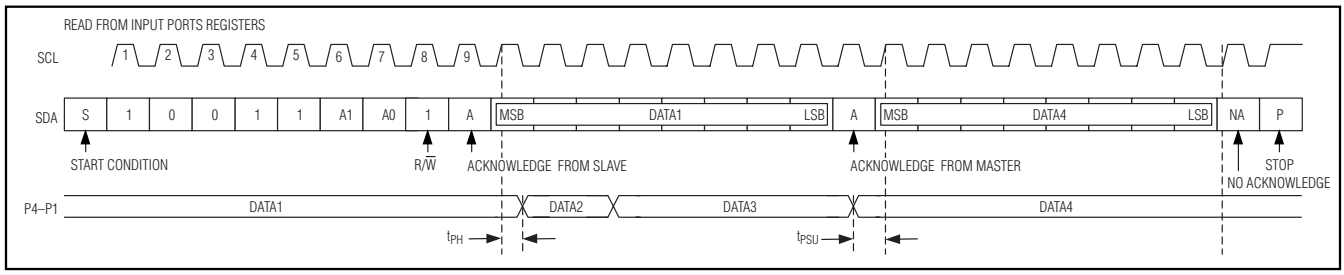


Figure 15. Read from Input Port Registers

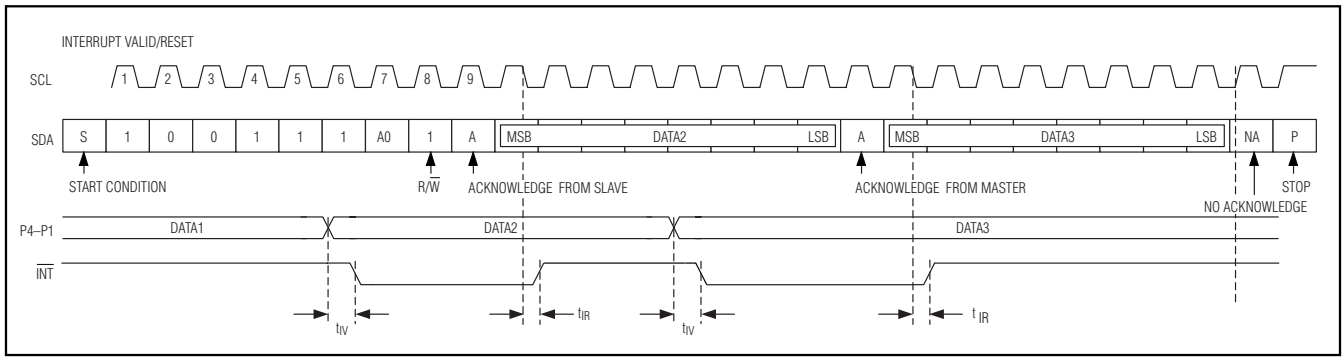


Figure 16. Interrupt and Reset Timing

same rules as for a write. Thus, a read is initiated by first configuring the MAX7306/MAX7307's command byte by performing a write (Figure 13). The master can now read n consecutive bytes from the MAX7306/MAX7307 with the first data byte being read from the register addressed by the initialized command byte (Figure 15). When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address has been autoincremented after the write (see Table 1).

Operation with Multiple Masters

If the MAX7306/MAX7307 are operated on a 2-wire interface with multiple masters, a master reading the MAX7306/MAX7307 should use a repeated start between the write that sets the MAX7306/MAX7307's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7306/MAX7307's address pointer, but before master 1 has read the data. If master 2 subsequently changes the MAX7306/MAX7307's address pointer, then master 1's delayed read can be from an unexpected location.

Bus Timeout

Clear device configuration register 0x27 bit D7 to enable the bus timeout function (see Table 2), or set it to disable the bus timeout function. Enabling the timeout feature resets the MAX7306/MAX7307 serial-bus interface when SCL stops either high or low during a read or write. If either SCL or SDA is low for more than

nominally 31ms after the start of a valid serial transfer, the interface resets itself and sets up SDA as an input. The MAX7306/MAX7307 then waits for another START condition.

Applications Information

Hot Insertion

Serial interfaces SDA, SCL (and AD0 for the MAX7306) remain high impedance with up to 5.5V asserted on them when the MAX7306/MAX7307 are powered down (V_{DD} = 0V), independent of the voltages on the port supply V_{LA}. When V_{DD} = 0V, or if V_{DD} falls below the MAX7306/MAX7307's reset threshold, all I/O ports become high impedance. Ports P2 through P4 remain high impedance to signals between 0V and the port supply V_{LA} for the MAX7307 and V_{DD} for the MAX7306. Port P1 goes high impedance to signals up to 5.5V. If a signal outside this range is applied to a port, the port's protection diodes clamp the input signal to V_{LA} or 0V, as appropriate. If the MAX7307's V_{LA} is lower than the input signal, the port pulls up V_{LA}, and the protection diode effectively powers any load on V_{LA} from the input signal. This behavior is safe if the current through each protection diode is limited to 10mA.

If it is important that I/O ports remain high impedance when all the supplies are powered down, including the port supply V_{LA}, then ensure that there is no direct or parasitic path for the MAX7306/MAX7307 input signals to drive current into either the regulator providing V_{LA} or other circuits powered from V_{LA}. One simple way to achieve this is with a series small-signal Schottky diode, such as the BAT54, between the port supply and the V_{LA} input.

I/O Level Translation

The open-drain output configuration of the ports allows them to level translate the outputs to lower (but not higher) voltages than the V_{LA} supply. An external pullup resistor converts the high-impedance, logic-high condition to a positive voltage level. Connect the resistor to any voltage up to V_{LA}. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Driving LED Loads

When driving LEDs, use a resistor in series with the LED to limit the LED current to no more than 25mA. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω)

V_{SUPPLY} is the supply voltage used to drive the LED (V)

V_{LED} is the forward voltage of the LED (V)

V_{OL} is the output low voltage of the MAX7306/MAX7307 when sinking I_{LED} (V)

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 20mA from a 5V supply, R_{LED} = (5 - 2.2 - 0.2) / 0.020 = 100Ω.

Driving Load Currents Higher than 25mA

The MAX7306/MAX7307 can sink current from loads drawing more than 25mA by sharing the load across multiple ports configured as open-drain outputs. Use at least one output per 25mA of load current; for example, drive a 90mA white LED with four ports.

The register structure of the MAX7306/MAX7307 allows only one port to be manipulated at a time. Do not connect ports directly in parallel because multiple ports cannot be switched high or low at the same time, which is necessary to share a load safely. Multiple ports can drive high-current LEDs because each port can use its own external current-limiting resistor to set that port's current through the LED.

Power-Supply Considerations

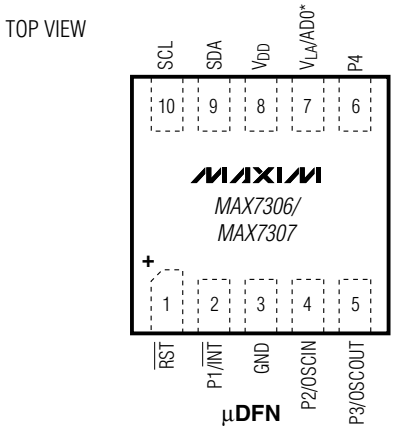
The MAX7306/MAX7307 operate with a V_{DD} power-supply voltage of 1.62V to 3.6V. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to the device. The port supply V_{LA} is connected to a supply voltage between 1.40V and 5.5V and bypassed with a 0.1µF capacitor as close as possible to the device. The V_{DD} supply and port supply are independent and can be connected to different voltages or the same supply as required.

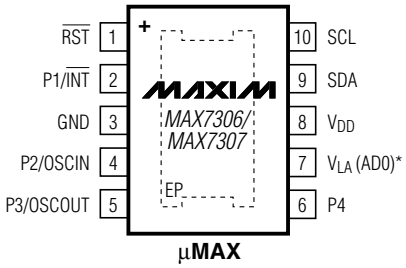
Power supplies V_{DD} and V_{LA} can be sequenced in either order or together.

For the MAX7307, when a push-pull port is acting as an input referenced to V_{CC}, make sure the VLA voltage is greater than V_{CC} - 0.3V.

SMBus/I²C Interfaced 4-Port, Level-Translating GPIOs and LED Drivers

Pin Configurations





EP = EXPOSED PADDLE

*AD0 FOR MAX7306
V_{LA} FOR MAX7307

Ordering Information (continued)

PART	TOP MARK	PIN-PACKAGE
MAX7306AUB+	AAAO	10 µMAX-EP*
MAX7307ALB+	AAK	10 µDFN (2mm x 2mm)
MAX7307AUB+	AAAN	10 µMAX-EP*

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10E+3	21-0109	90-0148
10 µDFN	L1022+1	21-0164	90-0006

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/07	Initial release	—
1	8/10	Updated *Driving LED Load* section	21

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